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EXAMINER	
STEELMAN, MARY J	

ART UNIT	PAPER NUMBER
2191	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/077,066	AU ET AL.	
	Examiner	Art Unit	
	Mary J. Steelman	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Per Applicant's request, claims 1, 11, 13, 21and 24 have been amended. Claims 1-25 are pending.

Claim Objections

2. In view of the claim amendments, the prior claim objections are hereby withdrawn.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5,970,439 to Levine et al.

Per claim 1:

An apparatus comprising:

-a full system monitor configured to monitor in real-time (i) one or more software variables down to change rates, (ii) one or more hardware registers down to cycle rates, and (iii) one or more firmware registers down to microcode word fetch rates in response to one or more trigger signals, wherein said one or more trigger signals is generated by a first comparator circuit.

(See FIGs. 4 & 7: performance monitoring invention; Col. 3, lines 58-60, "...analysis of system performance can be expanded beyond the boundaries of the processor to the entire data processing system (full system monitor)", col. 5, line 13, "a fetch unit...", col. 6, line 35, "fetch stage", col. 8, lines 46-54, "Performance monitor is a software accessible mechanism intended to provide detailed information with significant granularity concerning...instruction execution and storage control (software variables)...", col. 9, line 2, "event/signal selection to be recorded/counted (trigger signals)", col. 9, lines 8-9, "events that are selected for counting", col. 10, lines 41-44, "time period...data collected (cycle rates / fetch rates) has a context in terms of the number of minutes, hours, days, etc...", col. 10, lines 58-59, "identify particular areas in the software or hardware (hardware registers / firmware registers) where performance may be improved", col. 12, lines 6-9, "The counter selection fields...have as many bits necessary to specify the full domain of selectable events provided by a particular implementation" , col. 13, line 21, "programmable circuit (firmware)", col. 13, lines 48-49, "performance analyses may be made of operations within the entire system", col. 14, lines 55-61, "Each off-processor device might have its own way of controlling counting within its performance monitor. It might also have its own control registers...which would select events to count (comparator circuit)...", col. 16, lines 10-13, "...provides for **real time control and capture** of information related to signal analysis..." (emphasis added), col. 16, lines 21-22, "Programmable Logic Device...or Application Specific Integrated Circuit...(firmware)")

Levine did not explicitly disclose "software variables down to change rates, hardware registers down to cycle rates, and firmware registers down to microcode word fetch rates. He did however disclose (col. 8, lines 46-54) "Performance monitor is a software accessible mechanism intended to provide detailed information with significant granularity concerning...instruction execution and storage control..." Levine intended for the entire data processing system to be monitored. Levine mentions fetching instructions as an item of interest. Levine mentions software, hardware, and firmware may be involved. Levine disclosed cycle and change rates. Therefore, it would have been obvious, to modify Levine's invention to specifically disclose monitoring software variables down to change rates, hardware registers down to cycle rates, and firmware registers down to microcode word fetch rates because these are merely more specific details of features broadly disclosed in Levine's invention. The monitoring of these features provides (col. 3, lines 43-46) "a cost effective means to control and capture the information related to the system components"...to... "allow for a better analysis of system performance..."

Per claim 2:

-said apparatus is configured to monitor said one or more software variables, said hardware registers, and said firmware registers simultaneously.

(Col. 6, lines 27-29, "Processor achieves high performance by processing multiple instructions simultaneously...", col. 9, line 28-30, "Synchronization of the time base facility allows all processors in a multiprocessor system to initiate operation in synchronization." Simultaneous monitoring is available.)

Per claim 3:

-said apparatus comprises trace.

(Col. 9, line 2, "...allow for event/signal selection to be recorded/counted. (traced)")

Per claim 4:

-said apparatus is configured to generate one or more log files in response to said monitoring.

(Col. 9, line 2, ""...allow for event/signal selection to be recorded/counted. (record into log file)")

Per claim 5:

-said apparatus is configured to selectively monitor a specific one or more of said software variables, hardware registers, and firmware registers.

(Col. 3, lines 58-64, "...analysis of system performance can be expanded beyond the boundaries of the processor to the entire data processing system...create various analyses to be implemented with the various performance monitors within the devices in order to analyze various operational aspects (selectively monitor software variables, hardware registers, and firmware registers) of the data processing system" , col. 9, lines 1-4, "...registers are partitioned into bit fields that allow for event/signal selection to be recorded/counted. Selection (selectively monitor) of an allowable combination of events causes the counters to operate concurrently.")

Per claim 6:

-said apparatus further comprises software, hardware and firmware register coverage.

Col. 9, lines 1-4, ""...registers are partitioned into bit fields that allow for event/signal selection (of software, hardware or firmware registers) to be recorded/counted. Selection of an allowable combination of events causes the counters to operate concurrently.", col. 10, lines 58-59, "...identify particular areas (hardware / software / firmware register coverage) in the software or hardware where performance may be improved..", col. 13, line 21, "...programmable circuit...(firmware)")

Per claim 7:

-said apparatus is configured to selectively monitor one or more of said hardware and firmware registers to implement one or more of a verification self-test, a diagnostic method, and monitoring for firmware and software development.

(Col. 3, lines 60-64, "...designer of a data processing system can create various analyses (monitoring for development) to be implemented with the various performance monitors within the devices in order to analyze various operational aspects of the data processing system.")

Per claim 8:

-said apparatus further comprises one or more user defined start/stop triggers configured to start/stop one or more of said firmware registers, said hardware registers, and said software variables.

(Col. 10, lines 35-36, "...a predetermined number of events (triggers) is suitably used to select the stop point.", col. 17, lines 51-53, "This architecture allows any device (firmware registers,

said hardware registers, and said software variables) to signal a start counting condition or a stop counting condition (start / stop trigger)...")

Per claim 9:

-said monitor is configured to generate a time stamp of a monitor time.

(Col. 9, line 15-25, "The performance monitor is provided in conjunction with a time base facility...designates (generates) a precise point in time (time stamp)...includes a clock with a frequency...to provide a synchronized time base...", col. 10, lines 60-63, "...for those events being monitored that are time sensitive...the count number data is collected over a known number of elapsed cycles so that the data has a context in terms of a sampling period (a time stamp of a monitor time)...")

Per claim 10:

-said apparatus comprises monitoring hardware configured to connect to one or more internal busses of said system such that the monitoring is non-intrusive.

(Col. 9, lines 9-14, "Smaller or larger counters and register may be utilized to correspond to a particular processor and bus architecture (monitoring hardware configured to connect to one or more internal busses) or an intended application...", col. 13, lines 48-50, "...performance analyses may be made of operations within the entire system...by transferring performance monitoring signals across bus..." US Patent 5,691,920 to Levine (col. 1, line 64) which is incorporated by reference (col. 2, lines 20-21) disclosed (col. 3, line 58-59), "collected in a manner that is non-invasive to system operation...(monitoring is non-intrusive)")

Per claim 11:

-said apparatus comprises one or more comparators within said first comparator circuit configured to monitor one or more of an address, data, and a trigger trace.

(As an example of "comparator circuits configured to monitor" see col. 8, lines 32-43, which show comparisons done to indicate an instruction execution (address, data, or trigger situation). Col. 9, lines 48-56, "...a notification signal is sent to PM from time base facility when a predetermined bit is flipped. The PM then saves the machine state values in special purpose registers. In a different scenario, the PM uses a 'performance monitor' interrupt signaled by a negative counter...condition (comparator). The act of presenting the state information including operand and address data may be delayed...", lines 66-67, "The state of various execution units (address, data, and a trigger trace) are also saved.")

Per claim 12:

-said apparatus is configured to generate a trigger for trace and (i) said trigger is generated in response to one or more of a cycle and a register-delta and (ii) said register-delta comprises a difference between a previous value and a current value registered at one or more of said hardware and firmware registers.

(Col. 10, lines 24-35, "performance monitoring is implemented in a selected manner...through configuration of the performance monitor counters by the monitor mode control registers and performance monitoring data is collected...By adjusting the values...setting the values of the counters high enough so that an exception is signaled...a profile of system performance can be

obtained...", col. 12, lines 17-20, "The time from the start of the scenario is assumed to be available via system time services so that intervals of time (register-delta) may be used to correlate the different samples and different events.")

Per claim 13:

-said apparatus further comprises a CPU configured to (i) log said trace in response to polling the frequency of a read/write operation of said hardware and firmware register or said trigger signal. (A write operation (a 'store' instruction) is disclosed at col. 11, lines 20-24. Levine disclosed that the store instruction may involve a threshold value and (col. 11, lines 25-27), "A user may determine the number of times the threshold value is exceeded (frequency of a write operation) prior to the signaling of performance monitor interrupt", col. 13, lines 62-65, "signals control counting and can be used to inform CPU (CPU logs trace) or programmable circuit that device has a counter that has or is about to overflow (trigger to log)", col. 15, lines 41-43, "Software can set this bit to 1 (generate said poll) and then poll (log in response to a poll) the bit to determine whether an enabled condition or event (frequency of a read/write operation or a trigger signal) has occurred.")

Per claim 14:

-said apparatus is further configured to generate an analysis of time difference that corresponds to values monitored on said software variables and said hardware and firmware registers.

(Col. 10, lines 41-44, "...time period during which monitoring occurs is known...data collected has a context in terms of the number of minutes, hours, days, etc.", col. 10, lines 60-63, "events being monitored that are time sensitive...data has a context in terms of a sampling period.")

Per claim 16:

-said apparatus is configured to generate post-processing of said trace to assess register coverage.

(Col. 10, lines 45-59, "selected performance monitoring includes reconstructing a relationship among events, identifying...monitoring...The selected performance monitoring routine is completed and the collected data is analyzed (post processing of said trace)...identify particular areas in the software or hardware where performance may be improved.")

Per claim 17:

-said apparatus is further configured to monitor and calculate a frequency of use of each bit in said one or more hardware and firmware registers.

(Col. 9, lines 18-19, "The time base facility includes a clock with a frequency that is typically based upon the system bus...", col. 11, lines 57-65, "Bits are utilized to control interrupt signals triggered by PM...Bits are utilized to control the time or event-based transitions. The threshold value (X) is variably set by bits. Bit control counting enablement for PM....counting is enabled...counting is disabled...Bits are used for event selection, i.e., selection of signals to be counted..." A time based facility may be used to calculate frequency of bits counted. Also see col. 10, lines 58-63.)

Per claim 18:

-said monitoring hardware is configured to generate a time stamp of a monitor time.

(Col. 9, lines 25-28, "Predetermined bits...are selected for monitoring...such that the increment of time (timestamp) between monitored bit flips can be controlled", col. 10, lines 60-63, "for those events that are time sensitive...the count number of data is collected over a known number of elapsed cycles so that the data has a context in terms of a sampling period (timestamp)...")

Per claim 19:

-said apparatus is further configured to generate an analysis of filtering trace and capture that corresponds to one or more values monitored on said software variables and said hardware and firmware registers.

(Col. 3, lines 66-67, "signals sent between the processor and the various peripheral devices can be masked (filtering trace)", col. 11, lines 33-35, "bits...determine the scenarios under which counting is enabled...", col. 11, lines 39-41, "Bits indicate other specific conditions under which counting is frozen.", col. 11, lines 45-46, "PM represents the performance monitor marked bit...of a machine state register...")

Per claim 20:

-said apparatus is configured to define one or more windows configured to enable (i) said trace and (ii) a capture.

(Col. 11, lines 57-65, "Bits...are utilized to control interrupt signals triggered by PM...Bits...are utilized to control the time or event-based transitions. The threshold value...is variable set by

bits...Bit control counting enablement...Bits are used for event selection...(configure windows to enable trace and capture)"

Per claim 21:

-said apparatus is configured to filter bit levels of said hardware and firmware registers, such that remaining bits in said full system after said filtering can be assessed to achieve coverage.

(Col. 12, lines 6-9, "The counter selection fields...preferably have as many bits necessary to specify the full domain of selectable events (filtered bits used to assess performance coverage) provided by a particular implementation.")

Per claim 22:

-said apparatus comprises software defined monitor, trace and capture in hardware, software and firmware that correspond to trigger, log depth and trace windows.

Col. 4, lines 2-3, "...programming the various performance monitors...", col. 8, lines 47-48, "Performance monitor is a software-accessible mechanism intended to provide detailed information...", col. 11, line 33- col. 12, line 9, "bits...determine the scenarios under which counting is enabled...", col. 14, lines 22-23, "...a performance monitor interrupt, where the software determines the appropriate actions to take", col. 14, line 60-61, "...software would be used to initiate counting", col. 17, lines 51-53, "This architecture allows any device to signal a start counting condition or a stop counting condition from any other device", col. 18, lines 11-15, "This scheme allows for one processor to start counting after another processor reaches a certain state...This type of triggering could be used to have all processors start monitoring...")

Per claim 23:

-said apparatus is configured to generate a granularity of said time stamp between system events and register events that are monitored.

(Col. 8, lines 46-54, "Performance monitor is a software accessible mechanism intended to provide detailed information with significant granularity...", col. 9, lines 15-25, "The performance monitor is provided in conjunction with a time base facility which includes a counter that designates a precise point in time...includes a clock with a frequency...", col. 12, lines 17-20, "The time from the start of the scenario is assumed to be available via system time services so that intervals of time may be used to correlate the different samples and different events.")

Per claim 24:

A method for full system real-time monitoring comprising the steps of:

(Col. 19, line 31-col. 20, line 22, "...method (for full system monitoring)...")

(A) monitoring one or more software variables down to change rates;

(B) monitoring one or more hardware registers down to cycle rates;

(C) monitoring one or more firmware registers down to microcode word fetch rates;

(D) generating one or more trigger signals with a first comparator circuit to trigger said full system to monitor in real time.

(See rejection of limitations as addressed in claim 1 above.)

Per claim 25:

A computer readable medium containing one or more sets of computer executable instructions for performing the steps of claim 24.

(Col. 4, lines 31-33, "Fig. 7 illustrates a block diagram of a performance monitor configured (a computer readable medium containing instructions for performing...) in accordance with the present invention." See rejection of claims 1 and 24 above.)

Response to Arguments

5. Applicant's arguments filed 25 March 2005 have been fully considered but they are not persuasive.

(A) Applicant has argued, page 9, 2nd paragraph – page 10 2nd paragraph, that Levine does not teach a "full system monitor configured to monitor in real-time...software variable change rates, hardware register cycle rates, microcode word fetch rates...in response to one or more trigger signals generated by a first comparator circuit.

Examiner's Response: Examiner disagrees. Levine has disclosed (col. 8, line 46-col. 9, line 14) a performance monitor (a full system monitor)...intended to provide detailed information with significant granularity (variable change rates, register cycle rates, fetch rates) concerning the utilization of...instruction execution and storage control...Further included ...are monitor mode control registers...registers are partitioned into bit fields that allow for event/signal selection (trigger signals generated by comparator circuit) to be recorded/counted...counters and registers

may be utilized to correspond to a particular processor and bus architecture or an intended application..." Col. 10, lines 24-32, "...performance monitoring is implemented in a selected manner...through configuration of the performance monitor counters by the monitor mode control registers and performance monitoring data is collected...", col. 10, lines 45-52, "...selected performance monitoring includes reconstructing a relationship among events, identifying false triggering, identifying bottlenecks (register cycle rates), monitoring stalls (register cycle rates), monitoring idles (register cycle rates), determining the efficiency of operation of a dispatch unit (responding to a fetch instruction/ fetch rates), determining the effectiveness of branch unit operations, determining a performance penalty of misaligned data accesses (variable change rates), identifying a frequency of execution..." Although Levine failed to use the identical terms, Levine's invention serves as suitable prior art to the claimed invention.

6. Examiner maintains the rejection of claims 1-25.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Steelman, whose telephone number is (571) 272-3704. The examiner can normally be reached Monday through Thursday, from 7:00 AM to 5:30 PM If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached at (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mary Steelman

06/07/2005

WEI Y. ZHEN
PRIMARY EXAMINER